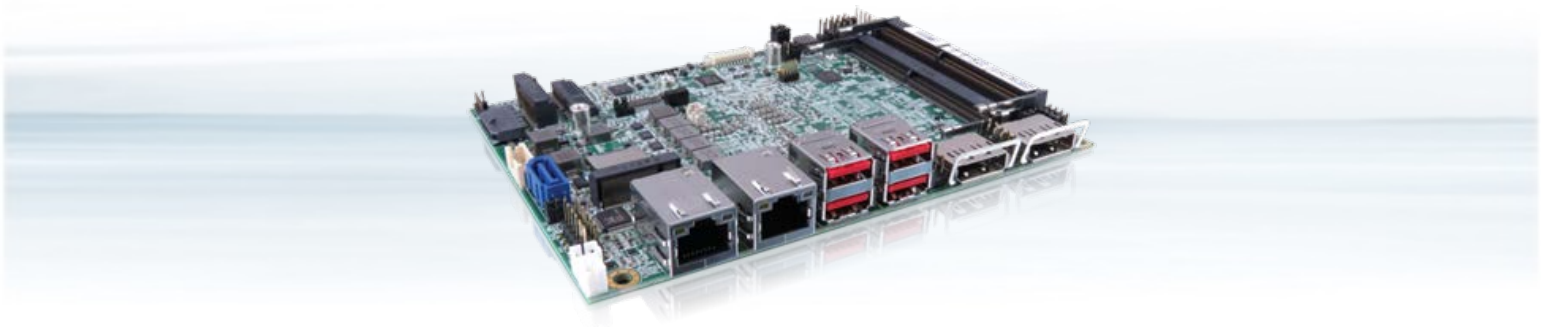
USER GUIDE



3.5"-SBC-WLU

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3.5"-SBC-WLU - USER GUIDE

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Revision History

Revision	Brief Description of Changes	Date of Issue	Author/ Editor
1.0	Initial Issue	2020-Feb-26	YS
1.1	Add a LPS power supply notice in Sec. 2.1	2020-Mar-31	YS

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Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit http://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

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1/ Introduction

This user guide describe the 3.5"-SBC-WLU board made by Kontron. This board will also be denoted 3.5"-SBC-WLU within this user guide.

Use of this user guide implies a basic knowledge of PC-AT hardware and software. This user guide focuses on describing the 3.5"-SBC-WLU board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the CPU board is either carried out automatically or manually by the user via the BIOS setup menus.

Latest revision of this user guide, datasheet, thermal simulations, BIOS, drivers, BSP's (Board Support Packages), mechanical drawings (2D and 3D) can de download from Kontron's Web Page.

2/ Installation Procedures

2.1. Installing the Board

NOTICE

ESD Sensitive Device!

Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.

- Wear ESD-protective clothing and shoes
- Wear an ESD-preventive wrist strap attached to a good earth ground
- Check the resistance value of the wrist strap periodically (1 MΩ to 10 MΩ)
- Transport and store the board in its antistatic bag
- Handle the board at an approved ESD workstation
- Handle the board only by the edges

To get the board running follow these steps. If the board shipped from KONTRON already has components like RAM and CPU cooler mounted, then skip the relevant steps below.

1. Turn off the PSU (Power Supply Unit)

NOTICE

Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise, components (RAM, LAN cards etc.) might get damaged. Make sure to use +12 V DC single supply only with suitable cable kit and PS-ON# active.

NOTICE

The power supply unit shall comply with the requirements as defined in IEC 62368-1 according Clause 6.2.2 to power source category PS2 "Limited Power Source".

2. Insert the DDR4 2400 / 2133 module(s)
   Be careful to push the memory module(s) in the slot(s) before locking the tabs.
3. Connecting interfaces
   Insert all external cables for hard disk, keyboard etc. A monitor must be connected in order to change BIOS settings.
4. Connect and turn on PSU
   Connect PSU to the board by the +12 V 3.0 mm pitch 1x4-pin wafer connector.
5. BIOS setup
   Enter the BIOS setup by pressing the <DEL> key during boot up.
   Enter "Exit Menu" and Load Setup Defaults.

To clear all BIOS setting, including Password protection, activate "Clear CMOS Jumper" for 10 sec (without power connected).

6. Mounting the board in chassis

NOTICE

When mounting the board to chassis etc. please note that the board contains components on both sides of the PCB that can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the board on a chassis, it is recommended to use screws with an integrated washer and a diameter of > 7 mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

2.2. Chassis Safety Standards

Before installing the 3.5"-SBC-WLU in the chassis, users must evaluate the end product to ensure compliance with the requirements of the IEC60950-1 safety standard:

- The board must be installed in a suitable mechanical, electrical and fire enclosure.
- The system, in its enclosure, must be evaluated for temperature and airflow considerations.
- The board must be powered by a CSA or UL approved power supply that limits the maximum input current.
- For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from and to the product shall be with SELV circuits only.
- Wires have suitable rating to withstand the maximum available power.
- The peripheral device enclosure fulfils the IEC60950-1 fire protecting requirements.

2.3. Lithium Battery Replacement

If replacing the lithium battery follow the replacement precautions stated in the notification below:

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

VORSICHT! Explosionsgefahr bei unsachgemäßem Austausch der Batterie.

- Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ
- Entsorgung gebrauchter Batterien nach Angaben des Herstellers

ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie.

- Remplacement seulement par le même ou un type équivalent recommandé par le producteur
- L'évacuation des batteries usagées conformément à des indications du fabricant

PRECAUCION! Peligro de explosión si la batería se sustituye incorrectamente.

- Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante
- Disponga las baterías usadas según las instrucciones del fabricante

ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering.

- Udskiftning må kun ske med batteri af samme fabrikat og type
- Levér det brugte batteri tilbage til leverandøren

ADVARSEL! Eksplosjonsfare ved feilaktig skifte av batteri.

- Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten
- Brukte batterier kasseres i henhold til fabrikantens instruksjoner

VARNING! Explosionsfara vid felaktigt batteribyte.

- Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren
- Kassera använt batteri enligt fabrikantens instruktion

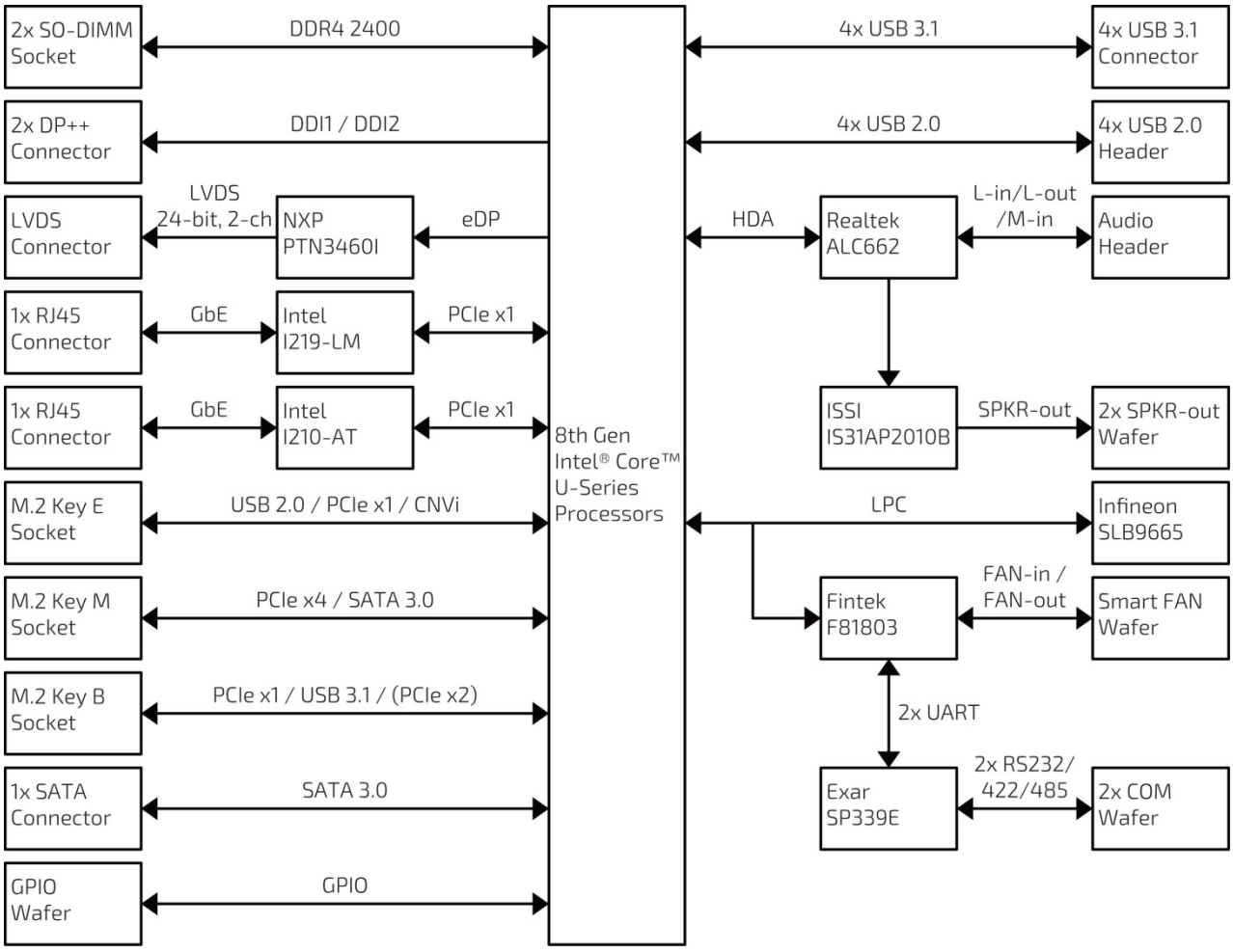
VAROITUS! Paristo voi räjähtää, jos se on virheellisesti asennettu.

- Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln
- Hävitä käytetty paristo valmistajan ohjeiden mukaisesti

3/ System Specifications

3.1. System Block Diagram

Figure 1: System Block Diagram 3.5"-SBC-WLU



3.2. Component Main Data

The table below summarizes the features of the 3.5"-SBC-WLU single board computer.

Table 1: Component Main Data

System	
Processor	8th Generation Intel® Core™ / Celeron® U-Series Processors
Memory	2x DDR4 SO-DIMM
Video	
Display Interface	1x LVDS 2x DP++ (on rear)
Multiple Display	Triple
Network Connection	
Ethernet	2x GbE LAN (RJ45 on rear, Intel® I219-LM, Intel® I210-AT)
Peripheral Connection	
USB	4x USB 3.1 (Type A on rear) 4x USB 2.0 (by header)
Serial Port	2x RS232/422/485 (by header)
Other I/Os	1x 8-bit DIO (by header)
Storage & Expansion	
Storage & Expansion	1x SATA 3.0 1x Micro SD Cage 1x M.2 Key B (Type 2242, mixed w/ PCIe x1 / USB 3.1) 1x M.2 Key E (Type 2230, mixed w/ PCIe x1 / USB 2.0, Intel CNVi support) 1x M.2 Key M (Type 2280 / 2242, mixed w/ PCIe x4 / SATA 3.0) 1x SIM Cage (Micro type, connected to M.2 Key B)
Power	
Input Voltage	DC 12 V
Connector	1x4-pin pitch 3.0 mm Wafer
Firmware	
BIOS	AMI uEFI BIOS w/ 256 Mb SPI Flash
Watchdog	Programmable WDT to generate system reset event
H/W Monitor	Voltages Temperatures
Real Time Clock	Processor integrated RTC
TPM	TPM 2.0 supported (Infineon SLB 9665)
System Control & Monitoring	
Front Panel Header	1x Header Reset Button, HDD LED & External Speaker 1x Header for Power Button, Power LED & SM bus 1x Header for M.2 Key B activity LED

System	
	1x Header for M.2 Key E activity LED
Cooling	
Fan	1x Wafer for System Fan
Software	
OS Support	Windows 10 Linux
Mechanical	
Dimension (L x W)	ECX (146 mm x 105 mm / 5.75" x 4.13")

3.3. Environmental Conditions

The 3.5"-SBC-WLU is compliant with the following environmental conditions. It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.

Table 2: Environmental Conditions

Operating Temperature	0 °C ~ 60 °C / 32 °F ~ 140 °F (Standard)
Storage Temperature	-20 °C ~ 80 °C / -4 °F ~ 176 °F (Standard)
Humidity	0 % ~ 95 %

3.4. Standards and Certifications

The 3.5"-SBC-WLU meets the following standards and certification tests.

Table 3: Standards and Certifications

CE Class B	TBD
FCC Class B	TBD

3.5. Processor Support

The 3.5"-SBC-WLU is designed to support 8th Generation Intel® Core™ / Celeron® U-Series Processors. The BGA CPU is remounted from factory. Kontron has defined the board versions as listed in the following table, so far all based on Embedded CPUs. Other versions are expected at a later date.

Table 4: Processor Support

Name	Core #	Speed	Turbo	Embedded	Cache	Socket	TDP	Tj
Core™ i7-8665UE	4	1.70 GHz	4.40 GHz	Yes	8M	FCBGA1528	15 W	100° C
Core™ i5-8365UE	4	1.60 GHz	4.10 GHz	Yes	6M	FCBGA1528	15 W	100° C
Core™ i3-8145UE	2	2.20 GHz	3.90 GHz	Yes	4M	FCBGA1528	15 W	100° C
Celeron® 4305UE	2	2.00 GHz	2.20 GHz	Yes	2M	FCBGA1528	15 W	100° C

Sufficient cooling must be applied to the CPU in order to remove the effect as listed as TDP (Thermal Design Power) in above table. The sufficient cooling is also depending on the worst case maximum ambient operating temperature and the actual worst case load of processor.

3.6. System Memory Support

The 3.5"-SBC-WLU has two DDR4 SO-DIMM sockets. The sockets support the following memory features:

- 2x DDR4 SO-DIMM 260-pin
- Dual-channel with 1x SO-DIMM per channel
- Up to 64 GB
- SPD timing supported
- ECC not supported

The installed DDR4 SO-DIMM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted, or the board may not be able to boot totally.

3.6.1. Memory Operating Frequencies

In all modes, the frequency of system memory is the lowest frequency of all the memory modules placed in the system. Each memory module's frequency can be determined through the SPD registers on the memory modules.

The table below lists the resulting operating memory frequencies based on the combination of SO-DIMMs and processor.

Table 5: Memory Operating Frequencies

SO-DIMM Type	Module Name	Memory Data Transfer (MT/s)	Processor System Bus Frequency (MHz)	Resulting Memory Clock Frequency (MHz)	Peak Transfer Rate (MB/s)
DDR4 2400	PC4-19200	2400	1200	300	19200
DDR4 2133	PC4-17000	2133	1067	267	17067

Memory modules have in general a much lower longevity than embedded motherboards, and therefore EOL of modules can be expected several times during lifetime of the motherboard.

As a minimum it is recommend using Kontron memory modules for prototype system(s) in order to prove stability of the system and as for reference.

For volume production you might request to test and qualify other types of RAM. In order to qualify RAM it is recommend configuring 3 systems running RAM Stress Test program in heat chamber at 60° C for a minimum of 24 hours.

3.7. On-board Graphics Subsystem

The 3.5"-SBC-WLU supports Intel® UHD Graphics technology for high quality graphics capabilities. All 3.5"-SBC-WLU versions support triple displays pipes.

Triple displays can be used simultaneously and be used to implement independent or cloned display configuration.

Table 6: Three-displays Configurations

Display 1	Display 2	Display 3	Max. Resolution (Px) at 60 Hz		
			Display 1	Display 2	Display 3
LVDS	DP++	DP++	1920 x 1200	4096 x 2304	4096 x 2304

3.8. Power Supply Voltage

In order to ensure safe operation of the board, the input power supply must monitor the supply voltage and shut down if the supply is out of range – refer to the actual power supply specification. Please note, in order to keep the power consumption to a minimal level, boards do not implement a guaranteed minimum load. The 3.5"-SBC-WLU board must be powered through the 3.0 mm pitch 1x4-pin wafer connector from a DC 12 V power supply.

NOTICE

Hot Plugging power supply is not supported. Hot plugging might damage the board.

The requirements to the supply voltages are as follows:

Table 7: Supply Voltages

Supply	Min.	Max.	Note
+12 V	11.4 V	12.6 V	Should be ±5 % tolerance

4/ Connector Locations

4.1. Top Side

Figure 2: Top Side

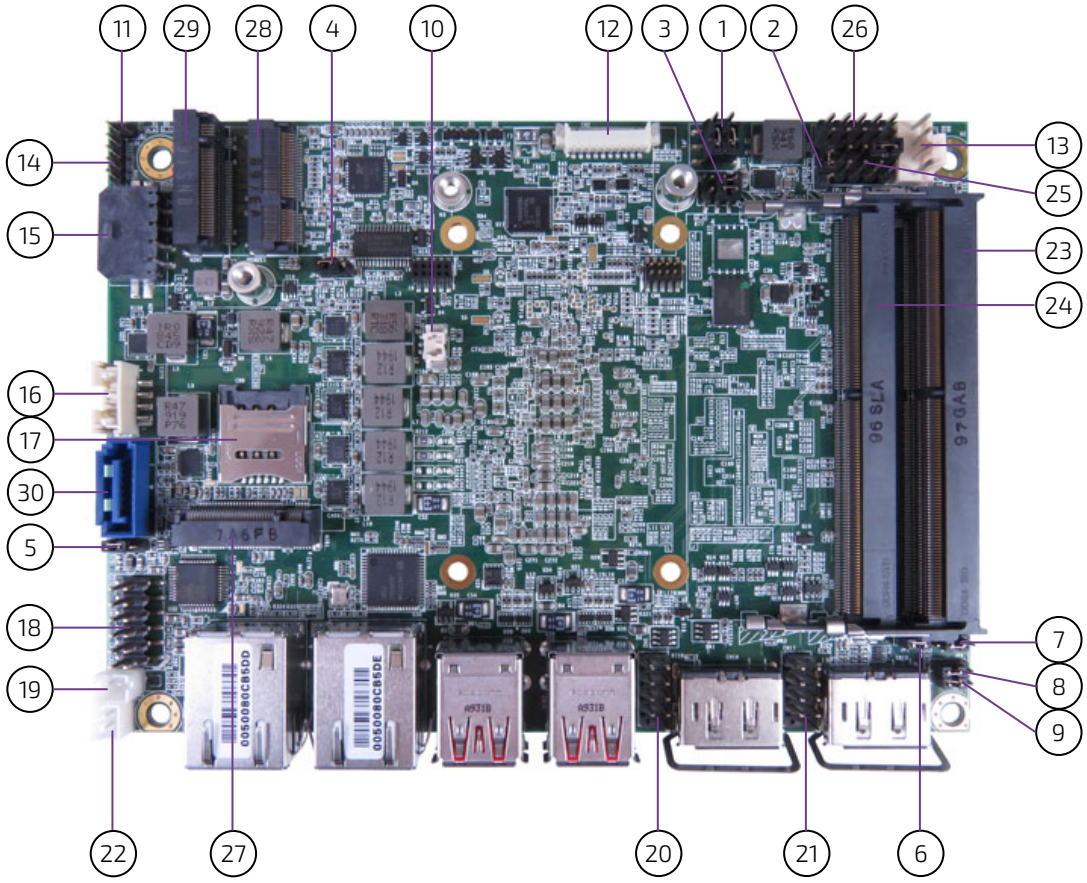


Table 8: Jumper List

Item	Designation	Description	See Chapter
1	JP1	LVDS Panel Power Selection	7.
2	JP2	LVDS Backlight Control Selection	7.
3	JP3	LVDS Backlight Enable Selection	7.
4	JP4	Integrated CNVi Selection for M2E1	7.
5	JP5	Flash Descriptor Security Override Selection	7.
6	JP6	AT / ATX Power Mode Selection	7.
7	JP7	Clear CMOS Selection	7.
8	JP9	USB Power Selection	7.
9	JP10	MFG Mode Selection	7.

Table 9: Top Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter
10	BAT1	RTC Power Input Wafer	7.1.2
11	CN1	Activity Indicator Header for M2B1	7.17
12	CN2	SDXC / DIO Header	7.12

Item	Designation	Description	See Chapter
13	CN3	FAN Wafer	7.2
14	CN4	Activity Indicator Header for M2E1	7.17
15	CN5	+12 V DC Power Input Wafer	7.1.1
16	CN8	+5 V DC HDD / SSD Power Output Wafer	7.4
17	CN9	Micro SIM Card Holder for M2B1	7.16
18	CN10	Audio Input / Output Header	7.7
19	CN11	Right Channel Audio AMP Output Wafer	7.6
20	CN16	USB 2.0 Port 6, 7 Header	7.5
21	CN17	USB 2.0 Port 8, 9 Header	7.5
22	CN20	Left Channel Audio AMP Output Wafer	7.6
23	DIMM1	DDR4 Channel 0 SO-DIMM Slot	3.6
24	DIMM2	DDR4 Channel 1 SO-DIMM Slot	3.6
25	FP1	Front Panel Header 1	7.8
26	FP2	Front Panel Header 2	7.8
27	M2B1	M.2 Key B 3042 Slot	7.13
28	M2E1	M.2 Key E 2230 Slot	7.14
29	M2M1	M.2 Key M 2242 / 2280 Slot	7.15
30	SATA1	SATA Port 0 Connector	7.3

4.2. Rear Side

Figure 3: Rear Side

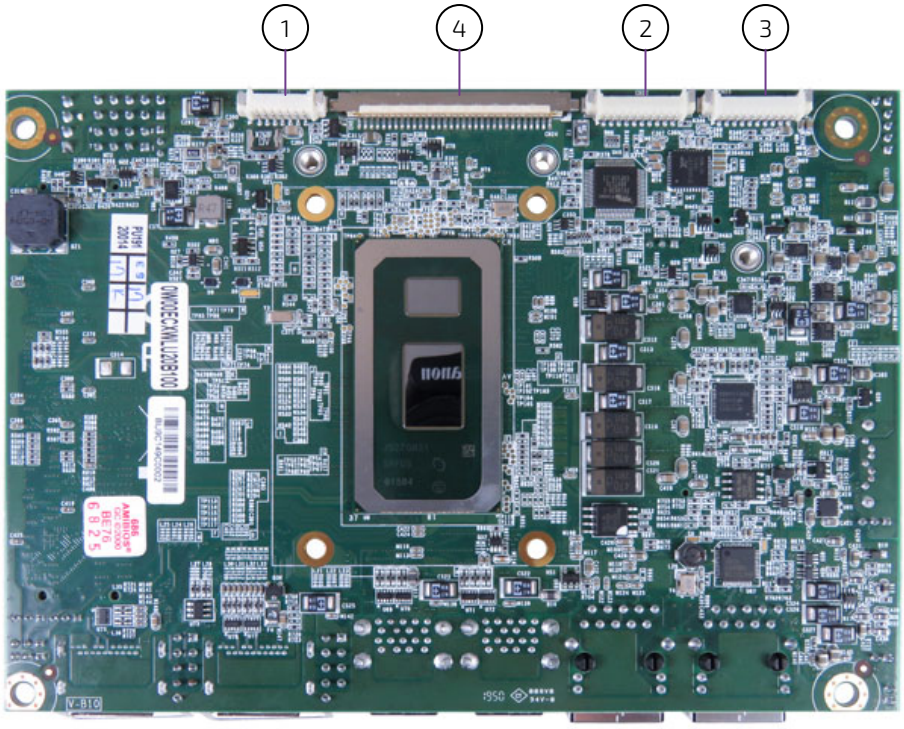


Table 10: Rear Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter
1	CN21	LVDS Backlight Power Wafer	7.11
2	CN22	RS232/422/485 COM2 Wafer	7.9
3	CN23	RS232/422/485 COM1 Wafer	7.9
4	CN24	24-bit / 2-ch LVDS Connector	7.10

4.3. Connector Panel Side

Figure 4: Connector Panel Side

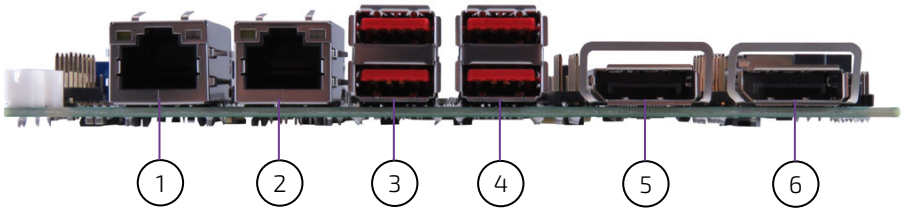


Table 11: Connector Panel Side Connector List

Item	Designation	Description	See Chapter
1	CN12	GbE LAN1 RJ45 Connector	6.2
2	CN13	GbE LAN2 RJ45 Connector	6.2
3	CN14	USB 3.1 Port 1, 2 Type A Connector	6.3
4	CN15	USB 3.1 Port 3, 4 Type A Connector	6.3
5	CN18	DP++ Port 2 Connector	6.1
6	CN19	DP++ Port 1 Connector	6.1

5/ Connector Definitions

The following defined terms are used within this user guide to give more information concerning the pin assignment and to describe the connector's signals.

Defined Term	Description
Pin	Shows the pin numbers in the connector
Signal	The abbreviated name of the signal at the current pin The notation "XX#" states that the signal "XX" is active low
Note	Special remarks concerning the signal
Designation	Type and number of item described
See Chapter	Number of the chapter within this user guide containing a detailed description

The abbreviation TBD is used for specifications that are not available yet or which are not sufficiently specified by the component vendors.

6/ I/O-Area Connectors

6.1. DP++ Connector (CN18 & CN19)

The DP++ (Dual-mode DisplayPort) connectors are based on standard DP female port.

Figure 5: DP Connector CN18, CN19

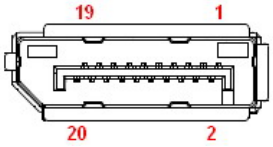


Table 12: Pin Assignment DP++ Connector CN18, CN19

Pin	Signal	Description	Note
1	ML_Lane0p	DisplayPort Lane 0 transmitter differential pair (+)	
2	GND	Ground	
3	ML_Lane0n	DisplayPort Lane 0 transmitter differential pair (-)	
4	ML_Lane1p	DisplayPort Lane 1 transmitter differential pair (+)	
5	GND	Ground	
6	ML_Lane1n	DisplayPort Lane 1 transmitter differential pair (-)	
7	ML_Lane2p	DisplayPort Lane 2 transmitter differential pair (+)	
8	GND	Ground	
9	ML_Lane2n	DisplayPort Lane 2 transmitter differential pair (-)	
10	ML_Lane3p	DisplayPort Lane 3 transmitter differential pair (+)	
11	GND	Ground	
12	ML_Lane3n	DisplayPort Lane 3 transmitter differential pair (-)	
13	Config1	Connected to ground, either directly or through a pulldown device	
14	Config2	Connected to ground, either directly or through a pulldown device	
15	AUX_CHp	DisplayPort Auxiliary channel differential pair (+)	
16	GND	Ground	
17	AUX_CHn	DisplayPort Auxiliary channel differential pair (-)	
18	Hot_Plug	DisplayPort hot plug detect	
19	GND	Ground	
20	DP_PWR	Power for connector	

6.2. Ethernet Connectors (CN12 & CN13)

The 3.5"-SBC-WLU supports two channels of 10/100/1000 Mbit Ethernet, which are based Intel® I219-LM and Intel® I210-AT controller respectively.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MByte and Category 5E, 6 or 6E with 1 Gbit LAN networks.

The signals for the Ethernet ports are as follows:

Figure 6: Ethernet Connectors CN12, CN13

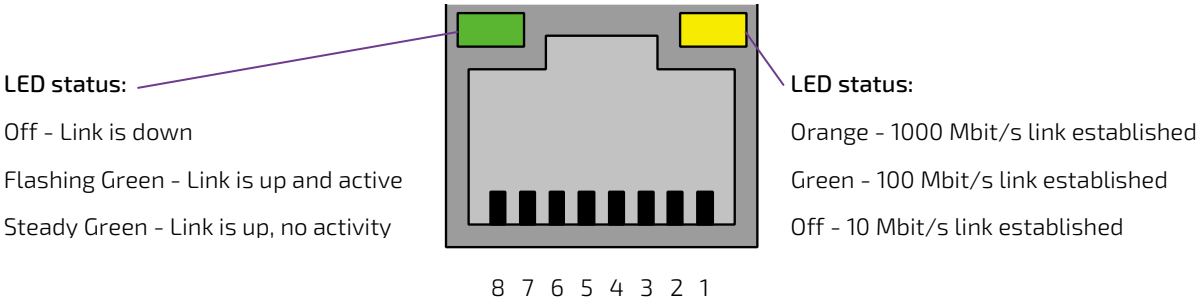


Table 13: Pin Assignment Ethernet Connector CN12, CN13

Pin	Signal	Note
1	TX1+	
2	TX1-	
3	TX2+	
4	TX3+	
5	TX3-	
6	TX2-	
7	TX4+	
8	TX4-	

Signal Description

Signal	Description
TX1+ / TX1-	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
TX2+ / TX2-	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
TX3+ / TX3-	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
TX4+ / TX4-	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.In MDI crossover mode, this pair acts as the BI_DC+/- pair.

'MDI' – media dependent Interface

6.3. USB Connectors (I/O Area)

The external I/O connector panel supports two dual USB 3.1 connectors.

USB 3.1 ports are backward compatible with USB 2.0.

Figure 7: USB 3.1 Connectors CN14 - Top & Bottom, CN15 - Top & Bottom

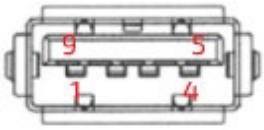


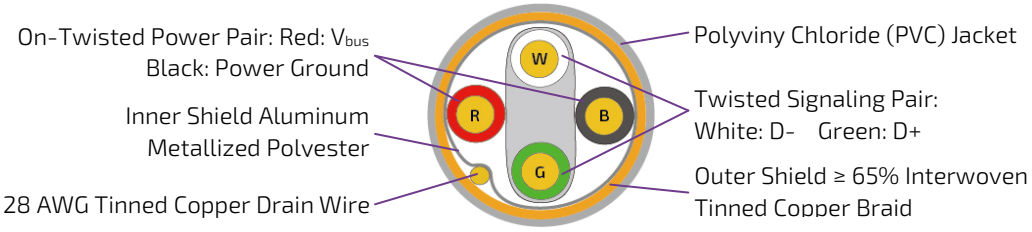
Table 14: Pin Assignment USB 3.1 / USB 2.0 Connectors CN14 - Top & Bottom, CN15 - Top & Bottom

Pin	Signal	Description	Note
1	+USB_VCC*	+5 V power supply for USB device	
2	USB_D-	USB 2.0 differential pair (-)	
3	USB_D+	USB 2.0 differential pair (+)	
4	GND	Ground	
5	USB_RX-	USB 3.1 receiver differential pair (-)	
6	USB_RX+	USB 3.1 receiver differential pair (+)	
7	GND	Ground	
8	USB_TX-	USB 3.1 transmitter differential pair (-)	
9	USB_TX+	USB 3.1 transmitter differential pair (+)	

*** The power source of +USBVCC can be selected by JP9.**

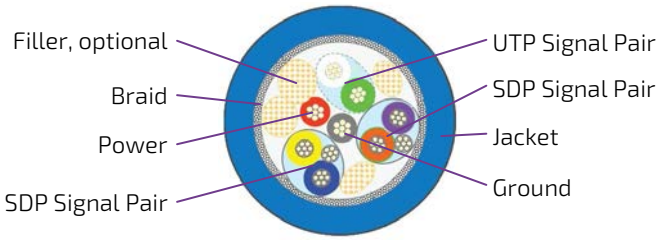
For HiSpeed rates it is required to use a USB cable, which is specified in USB 2.0 standard:

Figure 8: USB 2.0 High Speed Cable



For USB 3.1 cabling it is required to use only HiSpeed USB cable, specified in USB3.1 standard:

Figure 9: USB 3.1 High Speed Cable



7/ Internal Connectors

7.1. Power Connector

Power connector must be used to supply the board with +12 VDC (±5 %).

NOTICE

Hot plugging any of the power connector is not allowed.

Hot plugging might damage the board. In other words, turn off main supply etc. to make sure all the power lines are turned off when connecting to the motherboard.

7.1.1. Power Input Wafer (CN5)

The 1x4-pin 3.0 mm pitch power input wafer provides +12 V DC to the board.

Figure 10: Power Input Wafer CN5

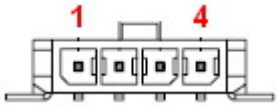


Table 15: Pin Assignment CN5

Pin	Signal	Description	Note
1	+12Vin	Power +12 V	
2	GND	Ground	
3	GND	Ground	
4	+12Vin	Power +12 V	

7.1.2. RTC Battery Power Input Wafer (BAT1)

The 1x2-pin 1.25 mm pitch RTC battery power input wafer is intended to be connected to the battery. The battery provides power to the system clock to retain the time when power is turn off.

Figure 11: RTC Battery Power Input Wafer BAT1

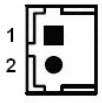


Table 16: Pin Assignment BAT1

Pin	Signal	Description	Note
1	+VRTC	Real-time clock backup battery input	
2	GND	Ground	

7.2. Fan Wafer (CN3)

The 1x4-pin 2.54 mm pitch system fan wafer (CN3) is used for the connection of the fan for the processor or system.

Figure 12: Fan Wafer CN3

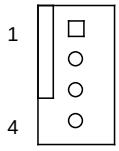


Table 17: Pin Assignment CN3

Pin	Signal	Description	Note
1	GND	Power supply ground signal	
2	+12V	+12 V power supply for fan	
3	SENSE	Sense input signal from the fan, for rotation speed supervision RPM (Rotations Per Minute).	
4	PWM	PWM output signal for FAN speed control	

7.3. SATA (Serial ATA) Port 0 Connector (SATA1)

The SATA connector supplies the data connection for the SATA hard disk and is SATA 3.0 compatible.

Figure 13: SATA Port 0 Connector SATA1

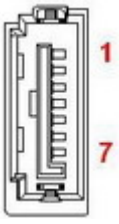


Table 18: Pin Assignment SATA1

Pin	Signal	Description	Note
1	GND	Ground	
2	TX+	Host transmitter differential signal pair (+)	
3	TX-	Host transmitter differential signal pair (-)	
4	GND	Ground	
5	RX-	Host receiver differential signal pair (-)	
6	RX+	Host receiver differential signal pair (+)	
7	GND	Ground	

7.4. HDD / SSD Power Output Wafer (CN8)

The 1x4-pin 2.0 mm pitch HDD / SSD power output wafer provides power to the SATA hard disk.

Figure 14: HDD / SSD Power Output Wafer CN8

Table 19: Pin Assignment CN8

Pin	Signal	Description	Note
1	+5V	+5 V power supply for HDD / SSD	
2	GND	Ground	
3	GND	Ground	
4	+5V	+5 V power supply for HDD / SSD	

7.5. USB Connectors (Internal) (CN16 & CN17)

The 10-pin 2.54 mm pitch USB port pin header CN16 & CN17 supports two USB 2.0 ports each.

Figure 15: USB 2.0 Port 6, 7 Pin Header CN16, Port 8, 9 Pin Header CN17

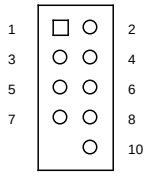


Table 20: Pin Assignment CN16, CN17

Pin	Signal	Description	Note
1	+USBVCC*	5 V supply. SB5V is supplied during power down to allow wakeup.	
2	+USBVCC*	5 V supply. SB5V is supplied during power down to allow wakeup.	
3	USB_DA-	USB 2.0 differential pair (-) for channel A	
4	USB_DB-	USB 2.0 differential pair (-) for channel B	
5	USB_DA+	USB 2.0 differential pair (+) for channel A	
6	USB_DB+	USB 2.0 differential pair (+) for channel B	
7	GND	Ground	
8	GND	Ground	
9	KEY		
10	GND	Ground	

* The power source of +USBVCC for CN16 and CN17 can be selected by JP9.

7.6. Audio AMP Output Wafer (CN11 & CN20)

The Speaker audio-out interface is available through the 2-pin 2.0 mm pitch wafers CN11 and CN20. These outputs are shared with the audio output (Line-out) signals of the audio pin header CN10.

Figure 16: Audio AMP Output Wafer CN11 (Right Channel), CN20 (Left Channel)

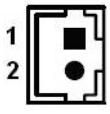


Table 21: Pin Assignment CN11, CN20

Pin	Signal	Description	Note
1	Speaker+	Speaker output (+)	
2	Speaker-	Speaker output (-)	

7.7. Audio Input / Output Pin Header (CN10)

The audio input / output pin header provides audio output (Line-Out), audio input (Line-In) and microphone (Mic-In) signals through the 12-pin 2.54 mm pitch wafer CN10. The audio output signals are shared with those of the speaker connectors CN11 & CN20.

Figure 17: Audio Input / Output Pin Header CN10

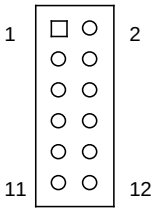


Table 22: Pin Assignment CN10

Pin	Signal	Description	Note
1	MIC-In_L	Microphone input left channel signal	
2	MIC-In_R	Microphone input right channel signal	
3	MIC-In_JD#	Microphone jack detection	
4	GND	Ground	
5	Line-In_L	Audio input left channel signal	
6	Line-In_R	Audio input right channel signal	
7	Line-In_JD#	Audio input jack detection	
8	GND	Ground	
9	Line-Out_L	Audio output left channel signal	
10	Line-Out_R	Audio output right channel signal	
11	Line-Out_JD#	Audio output jack detection	
12	GND	Ground	

7.8. Front Panel Pin Header (FP1 & FP2)

The 8-pin 2.54 mm pitch front panel pin header FP1 supplies signals for the reset button, storage LED and system warning speaker.

The 10-pin 2.54 mm pitch front panel pin header FP2 supplies signals for the power button, power LED, and SM Bus.

Figure 18: Front Panel 1 Pin Header FP1

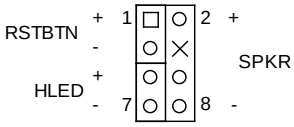


Table 23: Pin Assignment FP1

Pin	Signal	Description	Note
1	Reset Button +	System reset button (+)	
2	Speaker +	External system warning speaker (+)	
3	Reset Button -	System reset button (-)	
4	-	No connection	
5	HDD LED +	HDD activity LED (+). The LED lights up or flashes when data is ready from or written to the HDD.	
6	Internal Speaker -	Internal system warning speaker (-)	
7	HDD LED -	HDD activity LED (-).	
8	Speaker -	External system warning speaker (-)	

Internal Buzzer is enabled when Pin6-8 is shorted.

Figure 19: Front Panel 2 Pin Header FP2

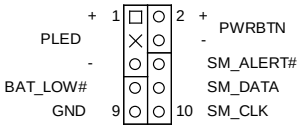


Table 24: Pin Assignment FP2

Pin	Signal	Description	Note
1	Power LED +	System Power LED (+). The LED lights up when users turn on the system power, and blinks when the system is in sleep mode.	
2	Power Button +	System power button (+). Pressing the power button turns the system on or puts the system in sleep or soft-off mode depending on the operating system settings. Pressing the power switch for more than four seconds while the system turns from ON to OFF.	
3	-	No connection	
4	Power Button -	System power button (-).	
5	Power LED -	System Power LED (-).	
6	-	No connection	
7	-	No connection	
8	SMBus Data	System management bus bidirectional data line	
9	GND	Ground	
10	SMBus Clock	System management bus bidirectional clock line	

7.9. Serial COM1 & COM2 Ports (CN23 & CN22)

The 10-pin 1.25 mm pitch serial COM wafer CN22 and CN23 provide RS232/422/485 connections.

Figure 20: Serial COM CN22, CN23

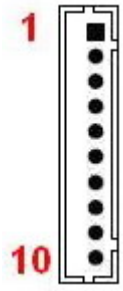


Table 25: Pin Assignment CN22, CN23

Pin	RS232 Signal	RS422 Signal	Half Duplex RS485 Signal	Full Duplex RS485 Signal	Note
1	DCD	TX-	DATA-	TX-	
2	DSR	-	-	-	
3	RXD	TX+	DATA+	TX+	
4	RTS	-	-	-	
5	TXD	RX+	-	RX+	
6	CTS	-	-	-	
7	DTR	RX-	-	RX-	
8	RI	-	-	-	
9	GND	GND	GND	GND	
10	+5V	+5V	+5V	+5V	

Table 26: Signal Description

Signal	Description
TXD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RXD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish communication link.
DSR	Data Set Ready, indicates that the modem etc. is ready to establish a communications link.
RTS	Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.
TX+/-	Transmitted Data differential pair sends data to the communications link.

Signal	Description
RX+/-	Received Data differential pair receives data from the communications link.
GND	Power Supply GND signal

7.10. LVDS Panel Connector (CN24)

The 30-pole 1.0 mm pitch JAE connector provides 24-bit, 2-channel LVDS panel connection.

Figure 21: LVDS Connector CN24

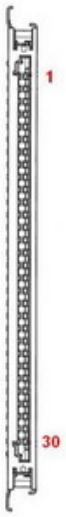


Table 27: Pin Assignment CN24

Pin	Signal	Description	Note
1	LVDSA_TX0-	LVDS Channel A Data 0 differential pair (-)	
2	LVDSA_TX0+	LVDS Channel A Data 0 differential pair (+)	
3	LVDSA_TX1-	LVDS Channel A Data 1 differential pair (-)	
4	LVDSA_TX1+	LVDS Channel A Data 1 differential pair (+)	
5	LVDSA_TX2-	LVDS Channel A Data 2 differential pair (-)	
6	LVDSA_TX2+	LVDS Channel A Data 2 differential pair (+)	
7	GND	Ground	
8	LVDSA_CLK-	LVDS Channel A clock differential pair (-)	
9	LVDSA_CLK+	LVDS Channel A clock differential pair (+)	
10	LVDSA_TX3-	LVDS Channel A Data 3 differential pair (-)	
11	LVDSA_TX3+	LVDS Channel A Data 3 differential pair (+)	
12	LVDSB_TX0-	LVDS Channel B Data 0 differential pair (-)	
13	LVDSB_TX0+	LVDS Channel B Data 0 differential pair (+)	
14	GND	Ground	
15	LVDSB_TX1-	LVDS Channel B Data 1 differential pair (-)	
16	LVDSB_TX1+	LVDS Channel B Data 1 differential pair (-)	
17	GND	Ground	
18	LVDSB_TX2-	LVDS Channel B Data 2 differential pair (-)	
19	LVDSB_TX2+	LVDS Channel B Data 2 differential pair (+)	
20	LVDSB_CLK-	LVDS Channel B clock differential pair (-)	
21	LVDSB_CLK+	LVDS Channel B clock differential pair (+)	

Pin	Signal	Description	Note
22	LVDSB_TX3-	LVDS Channel B Data 3 differential pair (-)	
23	LVDSB_TX3+	LVDS Channel B Data 3 differential pair (+)	
24	GND	Ground	
25	DDC_DATA	DDC channel Data	
26	VDDEN	Output Display Enable	
27	DDC_CLK	DDC Channel Clock	
28	VPNL *	+3.3 V / +5 V panel power supply	
29	VPNL *	+3.3 V / +5 V panel power supply	
30	VPNL *	+3.3 V / +5 V panel power supply	

* **Panel Power can be selected by JP1.**

7.11. LVDS Backlight Power Wafer (CN21)

The 7-pin 1.25 mm pitch wafer CN21 provides power supply for flat panel and its backlight inverter.

Figure 22: LVDS Backlight Power Wafer CN21

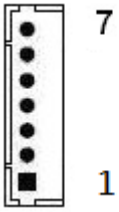


Table 28: Pin Assignment CN21

Pin	Signal	Description	Note
1	BL_EN***	Backlight Enable signal	
2	GND	Ground	
3	+VBKLT**	+5 V / +12 V backlight power supply	
4	+VBKLT**	+5 V / +12 V backlight power supply	
5	GND	Ground	
6	BL_ADJ_VOL*	Backlight Adjustment Voltage signal	
7	BL_ADJ_PWM*	Backlight Adjustment PWM (Pulse Width Modulation) signal	

* BL_ADJ can be selected by JP2.

** Backlight Power can be selected by JP1.

*** BL_EN can be selected by JP3.

7.12. Digital Input / Output Header (CN2)

The header CN2 supports 8-bit digital input / output signals to provide powering-on function of the connected devices.

Figure 23: Digital Input / Output Wafer CN2

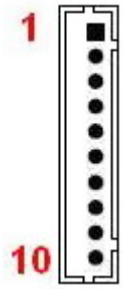


Table 29: Pin Assignment CN2

Pin	Signal	Description	Note
1	+5V	+5 V power supply	
2	DIO_0	Digital input / output channel 0	
3	DIO_1	Digital input / output channel 1	
4	DIO_2	Digital input / output channel 2	
5	DIO_3	Digital input / output channel 3	
6	DIO_4	Digital input / output channel 4	
7	DIO_5	Digital input / output channel 5	
8	DIO_6	Digital input / output channel 6	
9	DIO_7	Digital input / output channel 7	
10	GND	Ground	

7.13. M.2 Key B 3042 Slot (M2B1)

The 3.5"-SBC-WLU supports M.2 modules in format 3042 with Key B. The M.2 specification supports PCIe x1 and USB 3.1 signals as well as UIM signals connected to Micro SIM card holder CN9. The slot can be used to integrate WWAN communication to the mainboard.

Figure 24: M.2 Key B 2042 Slot M2B1

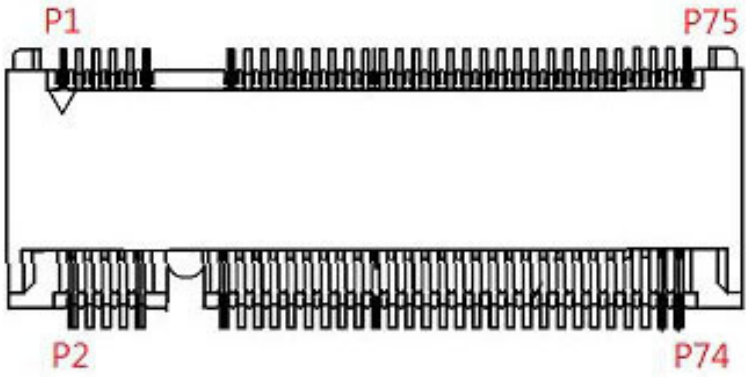


Table 30: Pin Assignment M2B1

Pin	Signal	Description	Note
1	-		
2	+3.3V	3.3 V power supply	
3	GND	Ground	
4	+3.3V	3.3 V power supply	
5	GND	Ground	
6	PWROFF#	M.2 module power enable	
7	USB-D+	USB 2.0 data differential pair (+)	
8	DISABLE#	Wireless disable	
9	USB-D-	USB 2.0 data differential pair (-)	
10	LED#	Device active signal	
11	GND	Ground	
12	KEY		
13	KEY		
14	KEY		
15	KEY		
16	KEY		
17	KEY		
18	KEY		
19	KEY		
20	-		
21	-		
22	-		
23	-		

Pin	Signal	Description	Note
24	-		
25	-		
26	-		
27	GND	Ground	
28	-		
29	USB3.0_RX-	USB 3.1 receiver differential pair (-)	
30	UIM_RESET*	SIM card reset	
31	USB3.0_RX+	USB 3.1 receiver differential pair (+)	
32	UIM_CLK*	SIM card clock	
33	GND	Ground	
34	UIM_DATA*	SIM card data	
35	USB3.0_TX-	USB 3.1 transmitter differential pair (-)	
36	UIM_PWR*	SIM card power	
37	USB3.0_TX+	USB 3.1 transmitter differential pair (+)	
38	-		
39	GND	Ground	
40	-		
41	PERn0	PCIe Lane 0 receiver pair (-)	
42	-		
43	PERp0	PCIe Lane 0 receiver pair (+)	
44	-		
45	GND	Ground	
46	-		
47	PETn0	PCIe Lane 0 transmitter pair (-)	
48	-		
49	PETp0	PCIe Lane 0 transmitter pair (+)	
50	PERST#	PCIe reset	
51	GND	Ground	
52	CLKREQ#	Reference clock request signal	
53	REFCLKn	PCIe reference clock pair (-)	
54	WAKE#	PCIe wake	
55	REFCLKp	PCIe reference clock pair (+)	
56	-		
57	GND	Ground	
58	-		
59	-		
60	-		
61	-		
62	-		
63	-		
64	-		
65	-		

Pin	Signal	Description	Note
66	SIM_DETECT	SIM card detect	
67	-		
68	SUSCLK	32.768 kHz clock supply input	
69	-		
70	+3.3V	3.3 V power supply	
71	GND	Ground	
72	+3.3V	3.3 V power supply	
73	GND	Ground	
74	+3.3V	3.3 V power supply	
75	-		

* These pins are connected to CN9 Micro SIM card holder directly.

7.14. M.2 Key E 2230 Slot (M2E1)

The 3.5"-SBC-WLU supports M.2 modules in format 2230 with Key E. The M.2 specification supports PCIe x1, USB 2.0 and / or CNVi signals. The slot can be used to integrate WLAN (Wi-Fi or CNVi Wi-Fi) and / or Bluetooth communication to the mainboard.

Figure 25: M.2 Key E 2230 Slot M2E1

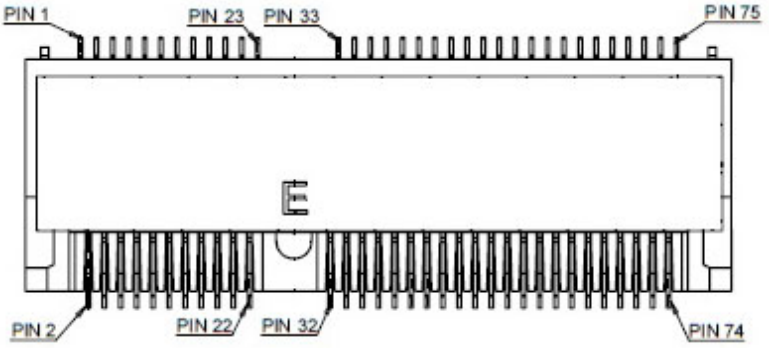


Table 31: Pin Assignment M2E1

Pin	Key E*		CNVi*		Note
	Signal	Description	Signal	Description	
1	GND	Ground	GND	Ground	
2	+3.3V	3.3 V power supply	+3.3V	3.3 V power supply	
3	USB_D+	USB 2.0 data diff. pair (+)	-		
4	+3.3V	3.3 V power supply	+3.3V	3.3 V power supply	
5	USB_D-	USB 2.0 data diff. pair (-)	-		
6	LED1#	Device active signal 1	LED1#	Device active signal 1	
7	GND	Ground	GND	Ground	
8	PCM_CLK	PCM synchronous data clock	-		
9	-		WGR_D1N	CNVio bus Rx Lane 1 (-)	
10	PCM_SYNC	PCM synchronous data sync	LCP_RSTN	RF companion (CRF) reset	
11	-		WGR_D1P	CNVio bus Rx Lane 1 (+)	
12	PCM_IN	PCM synchronous data input	-		
13	GND	Ground	GND	Ground	
14	PCM_OUT	PCM synchronous data output	CLKREQ0	Clock request	
15	-		WGR_D0N	CNVio bus Rx Lane 0 (-)	
16	LED2#	Device active signal 2	LED2#	Device active signal 2	
17	-		WGR_D0P	CNVio bus Rx Lane 0 (+)	
18	GND	Ground	GND	Ground	
19	GND	Ground	GND	Ground	
20	UART_WAKE#	UART wake-up	-		
21	-		WGR_CLKN	CNVio bus Rx clock (-)	
22	UART_RX	UART data input	BRI_RSP	BRI bus Rx	
23	-		WGR_CLKP	CNVio bus Rx clock (+)	

Pin	Key E*		CNVi*		Note
	Signal	Description	Signal	Description	
24	Key		Key		
25	Key		Key		
26	Key		Key		
27	Key		Key		
28	Key		Key		
29	Key		Key		
30	Key		Key		
31	Key		Key		
32	UART_TX	UART data output	RGI_DT	RGI bus Tx	
33	GND	Ground	GND	Ground	
34	UART_CTS	UART clear to send	RGI_RSP	RGI bus Rx	
35	PET0+	PCIe Lane 0 Tx pair (+)	-		
36	UART_RTS	UART request to send	BRI_DT	BRI bus Tx	
37	PET0-	PCIe Lane 0 Tx pair (-)	-		
38	Clink_RST	Wi-Fi CLINK host bus reset	-		
39	GND	Ground	GND	Ground	
40	Clink_DATA	Wi-Fi CLINK host bus data	-		
41	PER0+	PCIe Lane 0 Rx pair (+)	-		
42	Clink_CLK	Wi-Fi CLINK host bus clock	-		
43	PER0-	PCIe Lane 0 Rx pair (-)	-		
44	-		-		
45	GND	Ground	GND	Ground	
46	-		-		
47	REFCLK0+	PCIe reference clock pair (+)	-		
48	-		-		
49	REFCLK0-	PCIe reference clock pair (-)	-		
50	SUSCLK	32.768 kHz clock supply input	USUCLK	32.768 kHz clock supply input	
51	GND	Ground	GND	Ground	
52	PERST0#	PCIe reset	-		
53	CLKREQ0#	Reference clock request signal	-		
54	W_DISABLE2#	Wireless disable 2	W_DISABLE2#	Wireless disable 2	
55	PEWAKE0#	PCIe wake	-		
56	W_DISABLE1#	Wireless disable 1	W_DISABLE1#	Wireless disable 1	
57	GND	Ground	GND	Ground	
58	-		-		
59	-		WT_D1N	CNVio bus Tx Lane 1 (-)	
60	-		-		
61	-		WT_D1P	CNVio bus Tx Lane 1 (+)	
62	-		-		
63	GND	Ground	GND	Ground	
64	-		REFCLK0	Reference clock	

Pin	Key E*		CNVi*		Note
	Signal	Description	Signal	Description	
65	-		WT_D0N	CNVio bus Tx Lane 0 (-)	
66	-		-		
67	-		WT_D0P	CNVio bus Tx Lane 0 (+)	
68	-		-		
69	GND	Ground	GND	Ground	
70	-		-		
71	-		WT_CLKN	CNVio bus Tx clock (-)	
72	+3.3V	3.3 V power supply	+3.3V	3.3 V power supply	
73	-		WT_CLKP	CNVio bus Tx clock (+)	
74	+3.3V	3.3 V power supply	+3.3V	3.3 V power supply	
75	GND	Ground	GND	Ground	

* Integrated CNVi can be selected by the jumper JP4.

7.15. M.2 Key M 2242 / 2280 Slot (M2M1)

The 3.5"-SBC-WLU supports M.2 modules in format 2242 or 2280 with Key M. The M.2 specification supports PCIe x4 and SATA 3.0 signals. The slot can be used to integrate an M.2 PCIe x4 SSD (NVMe) or M.2 SATA SSD the mainboard.

Figure 26: M.2 Key M 2242 / 2280 Slot M2M1

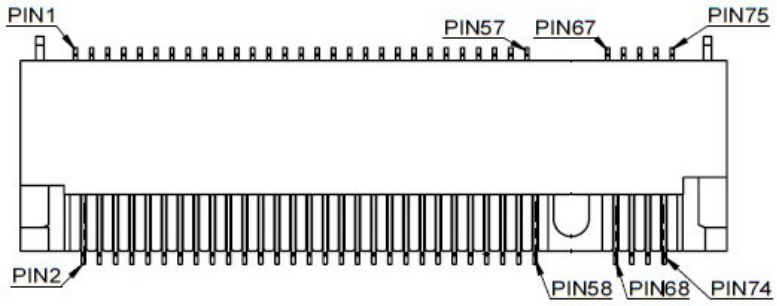


Table 32: Pin Assignment M2M1

Pin	Signal	Description	Note
1	GND	Ground	
2	+3.3V	3.3 V power supply	
3	GND	Ground	
4	+3.3V	3.3 V power supply	
5	PERn3	PCIe Lane 3 receiver pair (-)	
6	-		
7	PERp3	PCIe Lane 3 receiver pair (+)	
8	-	-	
9	GND	Ground	
10	DAS / DSS# / LED1#	Device active signal / disable staggered spin-up / LED	
11	PETn3	PCIe Lane 3 transmitter pair (-)	
12	+3.3V	3.3 V power supply	
13	PETp3	PCIe Lane 3 transmitter pair (+)	
14	+3.3V	3.3 V power supply	
15	GND	Ground	
16	+3.3V	3.3 V power supply	
17	PERn2	PCIe Lane 2 receiver pair (-)	
18	+3.3V	3.3 V power supply	
19	PERp2	PCIe Lane 2 receiver pair (-)	
20	-		
21	GND	Ground	
22	-		
23	PETn2	PCIe Lane 2 transmitter pair (-)	
24	-		
25	PETp2	PCIe Lane 2 transmitter pair (+)	
26	-		

Pin	Signal	Description	Note
27	GND	Ground	
28	-		
29	PERn1	PCIe Lane 1 receiver pair (-)	
30	-		
31	PERp1	PCIe Lane 1 receiver pair (+)	
32	-		
33	GND	Ground	
34	-		
35	PETn1	PCIe Lane 1 transmitter pair (-)	
36	-		
37	PETp1	PCIe Lane 1 transmitter pair (+)	
38	DEVSLP	Device sleep	
39	GND	Ground	
40	-		
41	PERn0 / SATA_B+	PCIe Lane 0 receiver pair (-) / SATA receiver pair (+)	
42	-		
43	PERp0 / SATA_B-	PCIe Lane 0 receiver pair (+) / SATA receiver pair (-)	
44	-		
45	GND	Ground	
46	-		
47	PETn0 / SATA_A-	PCIe Lane 0 transmitter pair (-) / SATA transmitter pair (-)	
48	-		
49	PETp0 / SATA_A+	PCIe Lane 0 transmitter pair (+) / SATA transmitter pair (+)	
50	PERST# / -	PCIe reset	
51	GND	Ground	
52	CLKREQ# / -	Reference clock request signal	
53	REFCLKn	PCIe reference clock pair (-)	
54	PEWAKE# / -	PCIe wake	
55	REFCLKp	PCIe reference clock pair (+)	
56	-		
57	GND	Ground	
58	-		
59	Key		
60	Key		
61	Key		
62	Key		
63	Key		
64	Key		
65	Key		
66	Key		
67	-		
68	SUSCLK	32.768 kHz clock supply input	

Pin	Signal	Description	Note
69	PEDET	PCIe detect	
70	+3.3V	3.3 V power supply	
71	GND	Ground	
72	+3.3V	3.3 V power supply	
73	GND	Ground	
74	+3.3V	3.3 V power supply	
75	GND	Ground	

7.16. Micro SIM Card Holder for M.2 Key B (CN9)

The Micro SIM card holder CN9 is intended to accommodate an Micro SIM card and connected to UIM signals on the M.2 Key B slot.

Figure 27: Micro SIM Card Holder CN9

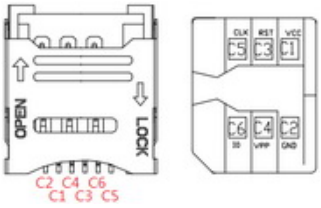


Table 33: Pin Assignment CN9

Pin	Signal	Description	Note
C1	VCC	Power +3.3 V	
C2	GND	Ground	
C3	RST	Reset signal	
C4	VPP	Programming voltage input	
C5	CLK	Clock signal	
C6	IO	Input or Output for serial data	

7.17. M.2 Key B / M.2 Key E Activity Indicator Header (CN1 & CN4)

The header CN1 is intended to connect M.2 Key B activity LED cable.

The pin header CN4 is intended to connect M.2 Key E activity LED cable.

Figure 28: M.2 Key B / M.2 Key E Activity Indicator Header CN1, CN4

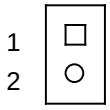


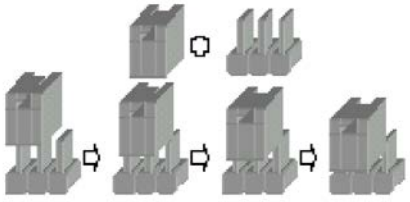
Table 34: Pin Assignment CN1, CN4

Pin	Signal	Description	Note
1	LED+		
2	LED-		

7.18. Switches and Jumpers

The product has several jumpers which must be properly configured to ensure correct operation.

Figure 29: Jumper Connector



For a three-pin jumper (see Figure 29), the jumper setting is designated “1-2” when the jumper connects pins 1 and 2. The jumper setting is designated “2-3” when pins 2 and 3 are connected and so on. You will see that one of the lines surrounding a jumper pin is thick, which indicates pin No.1.

To move a jumper from one position to another, use needle-nose pliers or tweezers to pull the pin cap off the pins and move it to the desired position.

7.18.1. LVDS Panel Power Selection (JP1)

The 2.54 mm pitch "LVDS Panel Power Selection" jumper (JP1) can be used to select LVDS panel and backlight power voltage.

Figure 30: LVDS Panel Power Selection JP1

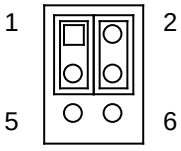


Table 35: Pin Assignment JP1

Jumper 1 Position		Description
Pin 1-3	Pin 3-5	
X	-	Backlight Power = +12 V
-	X	Backlight Power = +5 V
Jumper 2 Position		Description
Pin 2-4	Pin 4-6	
X	-	Panel Power = +3.3 V
-	X	Panel Power = +5 V

“X” = Jumper set (short) and “-” = jumper not set (open)

7.18.2. LVDS Backlight Control Selection (JP2)

The 2.0 mm pitch "LVDS Backlight Control Selection" jumper (JP2) can be used to select by which mode the brightness level in the LCD panel is controlled.

Figure 31: LVDS Backlight Control Selection JP2

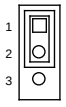


Table 36: Pin Assignment JP2

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	PWM Control Mode
-	X	Voltage Control Mode

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.3. LVDS Backlight Enable Selection (JP3)

The 2.0 mm patch "LVDS Backlight Enable Selection" jumper (JP3) can be used to select voltage level of backlight enable signal.

Figure 32: LVDS Backlight Enable Selection JP3

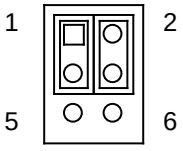


Table 37: Pin Assignment JP3

Jumper 1 Position		Description
Pin 1-3	Pin 3-5	
X	-	Backlight Enable Level = +3.3 V
-	X	Backlight Enable Level = +5 V
Jumper 2 Position		Description
Pin 2-4	Pin 4-6	
X	-	Backlight Enable High Active
-	X	Backlight Enable Low Active

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.4. Integrated CNVi Selection for M2E1 (JP4)

The 2.0 mm pitch "Integrated CNVi Selection for M2E1" jumper (JP4) can be used to select whether or not to enable CNVi device in M.2 Key E slot.

Figure 33: Integrated CNVi Selection JP4

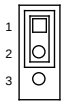


Table 38: Pin Assignment JP4

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Integrated CNVi Disabled
-	X	Integrated CNVi Enabled

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.5. Flash Descriptor Security Override Selection (JP5)

The 2.0 mm pitch "Flash Descriptor Security Override Selection" jumper (JP5) can be used to specify whether to override the flash descriptor.

Figure 34: Flash Descriptor Security Override Selection JP5

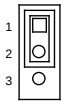


Table 39: Pin Assignment JP5

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Normal Operation
-	X	Flash Security Override

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.6. AT / ATX Power Mode Selection (JP6)

The 2.0 mm pitch jumper JP6 can be used to select AT power mode or ATX power mode.

Figure 35: AT / ATX Power Mode Selection JP6

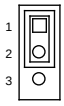


Table 40: Pin Assignment JP6

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	ATX Mode
-	X	AT Mode

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.7. Clear CMOS Selection (JP7)

The 2.0 mm pitch "Clear COMS Selection" jumper (JP7) can be used to reset the Real Time Clock (RTC) and drain RTC well.

The jumper has one position: Pin 1-2 mounted (default position) and Pin 2-3 mounted. More information on setting the "Clear CMOS Selection" jumper can be found in the following table.

Figure 36: Clear CMOS Selection JP7

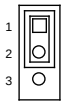


Table 41: Pin Assignment JP7

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Normal Operation (default position)
-	X	Clear CMOS (board does not boot with the jumper in this position)

"X" = Jumper set (short) and "-" = jumper not set (open)

Do not leave the jumper in position 2-3, otherwise if the power is disconnected, the battery will fully deplete within a few weeks.

7.18.8. USB Power Selection (JP9)

The 2.0 mm pitch "USB Power Selection" jumper (JP9) can be used to determine whether the USB ports are powered in the S4 / S5 state.

Figure 37: USB Power Selection JP9

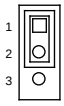


Table 42: Pin Assignment JP9

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	+5 V
-	X	+5 VSB

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.9. MFG Mode Selection (JP10)

The 2.0 mm pitch "MFG Mode Selection" jumper (JP10) can be used to rewrite Intel ME firmware onto another version.

Figure 38: MFG Mode Selection JP10

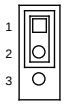


Table 43: Pin Assignment JP10

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Normal Operation
-	X	Enable MFG Mode

"X" = Jumper set (short) and "-" = jumper not set (open)

8/ BIOS

8.1. Starting the uEFI BIOS

The 3.5"-SBC-WLU is provided with a Kontron-customized, pre-installed and configured version of AMI Aptio® V uEFI BIOS. AMI BIOS firmware is based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the 3.5"-SBC-WLU.

The uEFI BIOS comes with a setup program that provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The setup program allows the accessing of various menus that provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A setup menu will appear.

The 3.5"-SBC-WLU uEFI BIOS setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the setup screens.

The following table provides information concerning the usage of these hot keys.

Table 44: Hotkeys Table

Signal	Description
<F1>	The <F1> key invokes the General Help window.
<->	The <Minus> key selects the next lower value within a field.
<+>	The <Plus> key selects the next higher value within a field.
<F2>	The <F2> key loads the previous values.
<F3>	The <F3> key loads the standard default values.
<F4>	The <F4> key saves the current settings and exit the uEFI BIOS setup.
<→> or <←>	The <Left/Right> arrows selects major setup menus on the menu bar. For example: Main, Advanced, Security, etc.
< ↑ > or < ↓ >	The <Up/Down> arrows selects fields in the current menu. For example: A setup function or a sub-screen.
<ESC>	The <ESC> key exits a major setup menu and enter the Exit setup menu. Pressing the <ESC> key in a sub-menu displays the next higher menu level.
<RERURN>	The <RETURN> key executes a command or select a submenu.

8.2. Starting the uEFI BIOS

The Setup utility features shows six menus in the selection bar at the top of the screen:

- Main
- Advanced
- Power
- Boot
- Security
- Save & Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

8.2.1. Main Setup Menu

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information. Additionally functions for setting the system time and date are offered.

Table 45: Main Setup Menu Sub-Screens and Functions

Function	Description
BIOS Information	Read only field. Displays information about the system BIOS
Memory Information	Read only field. Displays information about total memory
ME Information	Read only field. Displays information about Intel Management Engine (ME) version
Firmware Information	Code version and firmware information
System Date	Set System Date
System Time	Set System Time

Figure 39: BIOS Main Menu Screen System Data and Time

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Product Information					
Product Name	3.5-SBC-WLU				
BIOS Version	WHLUVEX.001 (x64)				
BIOS Build Date	01/08/2020				
ME Firmware SKU	Corporate SKU				
ME Firmware Version	12.0.49.1534				
CPU Information					
Intel® Core™ Processor i5-8365UE CPU @ 1.60 GHz					
Microcode Revision	CA				
Processor Cores	4 Core(s) / 8 Thread(s)				
Memory Information					
Total Size	4096 MB (DDR4)				
Frequency	2400 MHz				
Board Information					
UUID	01F94600-FF9E-13E0-8001-0050080CB60F			→ ←: Select Screen	
Serial #	BU9C129C0010			↑ ↓: Select Item	
LAN1 MAC Address	00:50:08:0C:B6:0F			Enter: Select	
LAN2 MAC Address	00:50:08:0C:B6:10			+/-: Change Opt.	
				F1: General Help	
System Date	[Wed 02/26/2020]			F2: Previous Values	
System Time	[15:54:55]			F3: Optimized Defaults	
				F4: Save & Exit	
Access Level	Administrator			ESC: Exit	
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Feature	Option	Description
System Date	[dd/mm/yyyy]	Set the Date. Use Tab to switch between Data elements.
System Time	[hh:mm:ss]	Set the Time. Use Tab to switch between Time elements.

8.2.2. Advanced Setup Menu

The Advanced setup menu provides sub-screens and functions for advanced configurations. The following sub-screen functions are included in the menu:

- LAN & Audio Configuration
- Display Configuration
- Super IO Configuration
- CPU Chipset Configuration
- NVMe Configuration
- SATA Configuration
- USB Configuration
- AMT Configuration
- Trusted Computing
- H/W Monitor
- Network Stack Configuration

NOTICE

Setting items on this screen to incorrect values may cause the system to malfunction.

Figure 40: BIOS Advanced Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Onboard LAN1 Controller		[Enabled]			
Onboard LAN2 Controller		[Enabled]			
Load I219 UNDI Driver		[Disabled]			
Load I210 UNDI Driver		[Disabled]			
Audio Controller		[Enabled]			
> Display Configuration					
> Super IO Configuration					
> CPU Chipset Configuration				→ ←: Select Screen	
> NVMe Configuration				↑ ↓: Select Item	
> SATA Configuration				Enter: Select	
> USB Configuration				+/-: Change Opt.	
> AMT Configuration				F1: General Help	
> Trusted Computing				F2: Previous Values	
> H/W Monitor				F3: Optimized Defaults	
				F4: Save & Exit	
> Network Stack Configuration				ESC: Exit	
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Feature	Option	Description
Onboard LAN1 Controller	[Disabled], [Enabled]	Select whether to enable or disable Onboard LAN1 Controller. Intel-i219.
Onboard LAN2 Controller	[Disabled], [Enabled]	Select whether to enable or disable Onboard LAN2 Controller. Intel-i210.
Load I219 UNDI Driver	[Disabled], [Enabled]	Select whether to load LAN UNDI Driver.
Load I210 UNDI Driver	[Disabled], [Enabled]	Select whether to load LAN UNDI Driver.
Audio Controller	[Disabled], [Enabled]	Select whether to enable or disable Audio Controller.

Figure 41: BIOS Advanced Menu - Display Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Display Configuration					
Primary Display		[IGFX]			
Internal Graphics*		[Enabled]			
Aperture Size		[256MB]			
DVMT Pre-Allocated		[32M]			
DVMT Total Gfx Mem		[256MB]		→ ←: Select Screen	
				↑ ↓: Select Item	
Active LVDS		[Enabled]		Enter: Select	
LVDS Panel Type		[1366x768 1CH]		+/-: Change Opt.	
LVDS Panel Color Depth		[18Bit]		F1: General Help	
PWM Backlight Control		[By External]		F2: Previous Values	
LVDS Backlight Control Mode		[PWM]		F3: Optimized Defaults	
LVDS Backlight Control - PWM**		127		F4: Save & Exit	
LVDS Backlight Control - Voltage***		[2.5 V]		ESC: Exit	
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* This item is selectable only when selecting PEG for the Primary Display.

** This item appears only when selecting PWM for the LVDS Backlight Control Mode.

*** This item appears only when selecting Voltage for the LVDS Backlight Control Mode.

Feature	Option	Description
Primary Display	[IGFX], [PEG]	Select which of IGFX / PEG Graphics device should be Primary Display.
Internal Graphics	[Disabled], [Enabled]	Keep IGFX enabled based on the setup options.
Aperture Size	[128MB], [256MB], [512MB], [1024MB], [2048MB]	Select the Aperture Size. Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.
DVMT Pre-Allocated	[32M], [64M], [4M], [8M], [12M], [16M], [20M], [24M], [28M], [32M], [32M/F7], [36M], [40M], [44M], [48M], [52M], [56M], [60M]	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	[128M], [256M], [MAX]	Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device.
Active LVDS	[Disabled], [Enabled]	Select the Active LVDS Configuration. [Disabled]: VBIOS does not enable LVDS. [Enabled]: VBIOS will enable LVDS.
LVDS Panel Type	[800x600 1CH], [1024x768 1CH], [1280x1024 2CH],	LVDS panel by selecting the appropriate setup item.

Feature	Option	Description
	[1366x768 1CH], [1366x768 2CH], [1600x1200 2CH], [1920x1080 2CH]	
LVDS Panel Color Depth	[18Bit], [24Bit]	LVDS panel color depth by appropriate setup item.
PWM Backlight Control	[By External], [By Internal]	CN21 LVDS Backlight Power Wafer Pin 2 output control [By External]: Control by external HW circuit. [By Internal]: Control by LBKL_CTL on the Intel Chipset.
LVDS Backlight Control Mode	[Voltage], [PWM]	CN21 LVDS Backlight Power output control [Voltage]: Pin 1 output [PWM]: Pin 2 output
LVDS Backlight Control - Voltage	[0.0 V], [0.5 V], [1.0 V], [1.5 V], [2.0 V], [2.5 V], [3.0 V], [3.5 V], [4.0 V], [4.5 V], [5.0 V]	Min: 0.0 V Max: 5.0 V

Figure 42: BIOS Advanced Menu - Super IO Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super IO Configuration					
> Serial Port 1 Configuration				→←: Select Screen	
> Serial Port 2 Configuration				↑ ↓: Select Item	
				Enter: Select	
				+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Figure 43: BIOS Advanced Menu - Super IO Configuration - Serial Port 1 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super Port 1 Configuration					
Serial Port		[Enabled]		→←: Select Screen	
Device Settings		IO=3F8h; IRQ=4;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
Serial Port 1 Type		[RS232]		F1: General Help	
RS485 Deplux Mode*		[Half Duplex]		F2: Previous Values	
RS485 Auto Flow Control*		[Disabled]		F3: Optimized Defaults	
RS485/422 Receiver Termination**		[Enabled]		F4: Save & Exit	
				ESC: Exit	
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* These items appear only when selecting RS485 for the Serial Port 1 Type.

** This item appears only when selecting RS485 or RS422 for the Serial Port 1 Type.

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=3F8h; IRQ=4;], [IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h;	Select an optional setting for Super IO device.

Feature	Option	Description
	IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	
Serial Port 1 Type	[RS232], [RS422], [RS485]	Select an appropriate type for Serial Port 1.
RS485 Duplex Mode	[Half Duplex], [Full Duplex]	Select an appropriate RS485 Duplex Mode.
RS485 Auto Flow Control	[Disabled], [Enabled]	Select whether to enable or disable RS485 Auto Flow Control.
RS485/422 Receiver Termination	[Disabled], [Enabled]	Select whether to enable or disable RS485/422 Receiver Termination.

Figure 44: BIOS Advanced Menu - Super IO Configuration - Serial Port 2 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super Port 2 Configuration					
Serial Port		[Enabled]		→ ←: Select Screen	
Device Settings		IO=2F8h; IRQ=3;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
Serial Port 2 Type		[RS232]		F1: General Help	
RS485 Deplux Mode*		[Half Duplex]		F2: Previous Values	
RS485 Auto Flow Control*		[Disabled]		F3: Optimized Defaults	
RS485/422 Receiver Termination**		[Enabled]		F4: Save & Exit	
				ESC: Exit	
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* These items appear only when selecting RS485 for the Serial Port 2 Type.

** This item appears only when selecting RS485 or RS422 for the Serial Port 2 Type.

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=2F8h; IRQ=3;], [IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	Select an optional setting for Super IO device.
Serial Port 2 Type	[RS232], [RS422], [RS485]	Select an appropriate type for Serial Port 2.
RS485 Duplex Mode	[Half Duplex], [Full Duplex]	Select an appropriate RS485 Duplex Mode.

Feature	Option	Description
RS485 Auto Flow Control	[Disabled], [Enabled]	Select whether to enable or disable RS485 Auto Flow Control.
RS485/422 Receiver Termination	[Disabled], [Enabled]	Select whether to enable or disable RS485/422 Receiver Termination.

Figure 45: BIOS Advanced Menu - CPU Chipset Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
CPU Chipset Configuration					
EIST		[Enabled]		→←: Select Screen	
Turbo Mode		[Enabled]		↑ ↓: Select Item	
Hyper-Threading		[Enabled]		Enter: Select	
VT-d		[Enabled]		+/-: Change Opt.	
Active Processor Cores		[All]		F1: General Help	
Intel (VMX) Virtualization Technology		[Enabled]		F2: Previous Values	
Intel Trusted Execution Technology		[Disabled]		F3: Optimized Defaults	
C states		[Enabled]		F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
EIST	[Disabled], [Enabled]	Select whether to enable or disable Enhanced Intel SpeedStep Technology.
Turbo Mode	[Disabled], [Enabled]	Select whether to enable or disable processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled).
Hyper-Threading	[Disabled], [Enabled]	Select whether to enable or disable Hyper-Threading Technology.
VT-d	[Disabled], [Enabled]	Select whether to enable or disable VT-d capability.
Active Processor Cores	[All], [1], [2], [3]	Select number of cores to enable in each processor package.
Intel (VMX) Virtualization Technology	[Disabled], [Enabled]	Select whether to enable or disable Intel Virtualization Technology. When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
Intel Trusted Execution Technology	[Disabled], [Enabled]	Select whether to enable or disable utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology. Changes require a full power cycle to take effect.
C states	[Disabled], [Enabled]	Select whether to enable or disable CPU Power Management. Allows CPU to go to C states when it's not 100% utilized.

Figure 46: BIOS Advanced Menu - NVMe Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
NVMe Configuration					
No NVMe Device Found				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
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Figure 47: BIOS Advanced Menu - SATA Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
SATA Configuration					
SATA Controller(s)		[Enabled]		→←: Select Screen	
SATA Mode Selection		[AHCI]		↑ ↓: Select Item	
				Enter: Select	
Serial ATA Port 1		Empty		+/-: Change Opt.	
Port 1		[Enabled]		F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
SATA Controller	[Enabled], [Disabled]	Select whether to enable or disable SATA Controller.
SATA Mode Selection	[AHCI], [Intel RST Premium With Intel Optane System Acceleration]	Determine how SATA controller(s) operate.
Port 1	[Disabled], [Enabled]	Select whether to enable or disable SATA Port 1.

Figure 48: BIOS Advanced Menu - USB Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
USB Configuration					
USB Devices:				→ ←: Select Screen	
1 Keyboard				↑ ↓: Select Item	
				Enter: Select	
Legacy USB Support		[Enabled]		+/-: Change Opt.	
XHCI Hand-off		[Disabled]		F1: General Help	
USB Mass Storage Driver Support		[Enabled]		F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
Legacy USB Support	[Enabled], [Disabled], [Auto]	Select whether to enable or disable Legacy USB support. AUTO option disables legacy support if no USB devices are connected.
XHCI Hand-off	[Enabled], [Disabled]	Select whether to enable or disable XHCI Hand-off function. This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	[Disabled], [Enabled]	Select whether to enable or disable USB Mass Storage Driver Support.

Figure 49: BIOS Advanced Menu - AMT Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
AMT Configuration					
AMT BIOS Features		[Enabled]		→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
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Feature	Option	Description
AMT BIOS Features	[Disabled], [Enabled]	Select whether to enable or disable AMT BIOS Features. When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup. Note: This option does not disable Manageability Features in FW.

Figure 50: BIOS Advanced Menu - Trusted Computing

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Configuration					
Security Device Support		[Disabled]			
No Security Device Found				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
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Feature	Option	Description
Security Device Support	[Disabled], [Enabled]	Select whether to enable or disable BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

Figure 51: BIOS Advanced Menu - H/W Monitor

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
PC Health Status					
> Smart FAN Configuration					
CPU Temperature		: +44 C			
Memory Temperature		: +30 C			
System Temperature		: +35 C			
CPU Fan Speed		: 7042 RPM		→ ←: Select Screen	
				↑ ↓: Select Item	
+VCORE		: +0.752 V		Enter: Select	
+VIN		: +12.000 V		+/-: Change Opt.	
+3VCC		: +3.328 V		F1: General Help	
+3VSB		: +3.344 V		F2: Previous Values	
+VBAT		: +3.168 V		F3: Optimized Defaults	
+5VA		: +5.088 V		F4: Save & Exit	
+3VA		: +3.344 V		ESC: Exit	
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Figure 52: BIOS Advanced Menu - H/W Monitor - Smart FAN Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Smart FAN Configuration					
CPU FAN Setting		[Manual]			
Manual Duty*		255		→ ←: Select Screen	
1st Boundary Temperature**		30		↑ ↓: Select Item	
1st FAN Speed**		50		Enter: Select	
2nd Boundary Temperature**		40		+/-: Change Opt.	
2nd FAN Speed**		100		F1: General Help	
3rd Boundary Temperature**		50		F2: Previous Values	
3rd FAN Speed**		150		F3: Optimized Defaults	
4th Boundary Temperature**		60		F4: Save & Exit	
4th FAN Speed**		200		ESC: Exit	
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* This item appears only when selecting Manual for CPU FAN Setting.

** These items appear only when selecting Smart for CPU FAN Setting.

Feature	Option	Description

Feature	Option	Description
CPU FAN Setting	[Manual], [Smart]	Switch the CPU FAN control mode.

Figure 53: BIOS Advanced Menu - Network Stack

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Network Stack		[Disabled]			
Ipv4 PXE Support*		[Disabled]			
Ipv4 HTTP Support*		[Disabled]		→←: Select Screen	
Ipv6 PXE Support*		[Disabled]		↑ ↓: Select Item	
Ipv6 HTTP Support*		[Disabled]		Enter: Select	
IPSEC Certificate*		[Enabled]		+/-: Change Opt.	
PXE boot wait time*		0		F1: General Help	
Media detect count*		1		F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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* These items appear only when enbling Network Stack.

Feature	Option	Description
Network Stack	[Disabled], [Enabled]	Select whether to enable or disable UEFI network stack.
Ipv4 PXE Support	[Disabled], [Enabled]	Select whether to enable or disable Ipv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
Ipv4 HTTP Support	[Disabled], [Enabled]	Select whether to enable or disable Ipv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
Ipv6 PXE Support	[Disabled], [Enabled]	Select whether to enable or disable Ipv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
Ipv6 HTTP Support	[Disabled], [Enabled]	Select whether to enable or disable Ipv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
IPSEC Certificate	[Disabled], [Enabled]	Select whether to enable or disable IPSEC certificate for Ikev.

8.2.3. Power Setup Menu

The Power setup menu provides functions and a sub-screen for power configurations. The following sub-screen function is included in the menu:

- WatchDog Timer Configuration

Figure 54: BIOS Power Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Power Configuration					
ACPI Sleep State		[S3 (Suspend to RAM)]			
Restore AC Power Loss		[Power Off]		→ ←: Select Screen	
Power Saving Mode		[Disabled]		↑ ↓: Select Item	
				Enter: Select	
Resume Event Control				+/-: Change Opt.	
Resume By LAN Device		[Disabled]		F1: General Help	
Resume By Ring Device		[Disabled]		F2: Previous Values	
Resume By RTC Alarm		[Disabled]		F3: Optimized Defaults	
> WatchDog Timer Configuration				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
ACPI Sleep State	[S3 (Suspend to RAM)]	Select whether to enable or disable suspend function and determine an appropriate suspend mode.
Restore AC Power Loss	[Power Off], [Power On], [Last State]	This field controls whether the system will stay on after AC power is removed and then restored. Select [Power Off] if you want the system to remain off after power restored. Select [Power On] if you use a power strip to turn the system on.
Power Saving Mode	[Disabled], [EUP Enabled]	Select whether to enable Power Saving Mode. [EUP Enabled]: The system will enter to EUP Power Saving Mode during power off. [DeepSx Enabled]: The system will enter to DeepSx Power Saving Mode during S4 / S5 power off. [Disabled]: Disables function of all Power Saving Mode.
Resume By LAN 1 Device	[Disabled], [Enabled]	Select whether to enable or disable Wake from LAN Device.
Resume By Ring Device	[Disabled], [Enabled]	Select whether to enable or disable Wake from Ring Device.
Resume By RTC Alarm	[Disabled], [Enabled]	Select whether to enable or disable Wake Up on Alarm, to turn on your system on a special day of the month.

Figure 55: BIOS Power Setup Menu - WatchDog Timer Configuration

BIOS SETUP UTILITY

Main	Advanced	Power	Boot	Security	Save & Exit
WatchDog Timer Configuration					
WDT Function		[Disabled]		→ ←: Select Screen	
WDT Count Mode*		[Second]		↑ ↓: Select Item	
WDT Timer*		30		Enter: Select	
				+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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* These items appear only when enbling WDT Function.

Feature	Option	Description
WDT Function	[Disabled], [Enabled]	Select whether to enable or disable WatchDog Timer function.
WDT Count Mode	[Second], [Minute]	Select WatchDog Count Mode: Second or Minute.

8.2.4. Boot Setup Menu

The boot setup menu lists the for boot device priority order, that is generated dynamically.

Figure 56: BIOS Boot Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Boot Configuration					
Full Screen LOGO Display		[Disabled]			
Setup Prompt Timeout		1		→ ←: Select Screen	
Bootup NumLock State		[On]		↑ ↓: Select Item	
				Enter: Select	
CSM Support		[Disabled]		+/-: Change Opt.	
Boot Option Filter		[UEFI Only]		F1: General Help	
				F2: Previous Values	
Boot Option Priorities				F3: Optimized Defaults	
Boot Option #1		[UEFI: Built-in EFI Shell]		F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
Full Screen LOGO Display	[Disabled], [Enabled]	Select whether to enable or disable to display logo screen.
Bootup NumLock State	[On], [Off]	This field indicates the state of the NumLock feature of the keyboard after Startup. [On]: The keys on the keypad will act as numeric keys. [Off]: The keys on the keypad will act as cursor keys.
CSM Support	[Enabled], [Disabled]	Select whether to enable or disable CSM support.
Boot Option Filter	[UEFI only]	This option controls Legacy / UEFI ROMs priority.
Boot Option #1	[UEFI: Built-in EFI Shell], [Disabled]	Select an option for first boot device.

8.2.5. Security Setup Menu

The Security setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The 3.5"-SBC-WLU provides no factory-set passwords.

NOTICE

If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.

Figure 57: BIOS Security Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Password Description If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights The password length must be in the following range:					
Minimum Length		3		→ ←: Select Screen	
Maximum length		20		↑ ↓: Select Item	
				Enter: Select	
Administrator Password				+/-: Change Opt.	
User Password				F1: General Help	
				F2: Previous Values	
> Secure Boot				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Description
Administrator Password	Set administrator password
User Password	Set user password

If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.

Password length requirements are maximum 20 characters and minimum 3 characters.

8.2.5.1. Remember the password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not know, contact Kontron Support for further assistance.

HDD security passwords cannot be cleared using the above method.

8.2.6. Save & Exit Setup Menu

The exit setup menu provides functions for handling changes made to the UEFI BIOS settings and the exiting of the setup program.

Figure 58: BIOS Save & Exit Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Save Changes and Reset Discard Changes and Reset					
Save Options Save Changes Discard Changes Restore Defaults				→ ←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
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Feature	Description
Save Changes and Exit	Exit system setup after saving the changes. Once you are finished making your selections, choose this option from the Exit menu to ensure the values you selected are saved to the CMOS RAM. The CMOS RAM is sustained by an onboard backup battery and stays on even when the PC is turned off. When you select this option, a confirmation window appears. Select [Yes] to save changes and exit.
Discard Changes and Exit	Exit system setup without saving any changes. Select this option only if you do not want to save the changes that you made to the Setup program. If you made changes to fields other than system date, system time, and password, the BIOS asks for a confirmation before exiting.
Save Changes	Save changes done so far to any of the setup values. This option allows you to save the selections you made. After selecting this option, a confirmation appears. Select [Yes] to save any changes.
Discard Changes	Discards changes done so far to any of the setup values. This option allows you to discard the selections you made and restore the previously saved values. After selecting this option, a confirmation appears. Select [Yes] to discard any changes and load the previously saved values.
Restore Defaults	Restore Default values for all the setup values. This option allows you to load optimal default values for each of the parameters on the Setup menus, which will provide the best performance settings for your system. The F9 key can be used for this operation.

Appendix A: List of Acronyms

The following table does not contain the complete acronyms used in signal names, signal type definitions or similar. A description of the signals is included in the I/O Connector and Internal connector chapters within this user guide.

Table 46: List of Acronyms

2D	Two-Dimensional
3D	Three-Dimensional
AT	Advanced Technology
ATX	Advanced Technology eXtended
BGA	Ball Grid Array
BIOS	Basic Input / Output System
BSP	Board Support Package
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DC	Direct Current
DDC	Display Data Channel
DIO	Digital Input / Output
DP	DisplayPort
ECC	Error-Correcting Code
EEE	Electrical and Electronic Equipment
EOS	Electrical OverStress
ESD	ElectroStatic Discharge
GbE	Gigabit Ethernet
HDD	Hard Disk Drive
HDMI	High Definition Multimedia Interface
LAN	Local Area Network
LED	Light Emitting Device
LVDS	Low-Voltage Differential Signaling
ME F/W	Management Engine Firmware
mPCIe	mini Peripheral Component Interconnect express
NGFF	Next Generation Form Factor
PC-AT	Personal Computer - Advanced Technology
PCB	Printed Circuit Board
PSU	Power Supply Unit
PVC	PolyViny Chloride
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital memory card
SDP	Serial Download Protocol
SELV	Safety Extra-Low Voltage
SIM	Subscriber Identity Module
SMBus	System Management Bus
SoC	System on Chip
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
TDP	Thermal Design Power
TPM	Trusted Platform Module
UEFI	Unified Extensible Firmware Interface
USB	Universal Serial Bus
UTP	Update Transfer Protocol
VGA	Video Graphics Array
WDT	WatchDog Timer
WEEE	Waste Electrical and Electronic Equipment

About Kontron

Kontron is a global leader in Embedded Computing Technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall. For more information, please visit: www.kontron.com

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